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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,320	04/01/2004	Ramadas Lakshmikanth Pai	15472US02	9138
	7590 01/05/201 S HELD & MALLOY,	EXAMINER		
500 WEST MADISON STREET SUITE 3400			HOLDER, ANNER N	
CHICAGO, IL	60661		ART UNIT	PAPER NUMBER
			2483	
			MAIL DATE	DELIVERY MODE
			01/05/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Application No.	Applicant(s)			
Office Action Summary		10/816,320	PAI ET AL.			
		Examiner	Art Unit			
		ANNER HOLDER	2483			
Period fo	The MAILING DATE of this communication app or Reply	ears on the cover sheet with the c	orrespondence ad	ldress		
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1)  ズ	Responsive to communication(s) filed on 20 Oc	ctober 2010.				
· ·		action is non-final.				
3)	Since this application is in condition for allowan		secution as to the	e merits is		
-,	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
	•	,				
Disposit	ion of Claims					
4) 🛛	Claim(s) <u>1,2,4-9,11-15 and 17-21</u> is/are pendin	g in the application.				
	4a) Of the above claim(s) is/are withdraw	vn from consideration.				
5)	Claim(s) is/are allowed.					
6)🛛	Claim(s) <u>1,2,4-9,11-15 and 17-21</u> is/are rejecte	d.				
7)	Claim(s) is/are objected to.					
8)	Claim(s) are subject to restriction and/or	election requirement				
∪/∟	are subject to restriction and/or	olootion roquiromont.				
Applicat	ion Papers					
9) 🗆	The specification is objected to by the Examiner	·.				
10)⊠ The drawing(s) filed on <u>01 April 2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
,	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.321(d).					
441				` ,		
11)	The oath or declaration is objected to by the Ex-	aminer. Note the attached Office	Action or form Pi	10-152.		
Priority ι	under 35 U.S.C. § 119					
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No.</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>						
2) Notice 3) Infor	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO/SB/08) er No(s)/Mail Date	4)  Interview Summary Paper No(s)/Mail Da 5)  Notice of Informal P 6)  Other:	ite			

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## **DETAILED ACTION**

## Response to Arguments

1. Applicant's arguments filed 10/20/10 have been fully considered but they are not

persuasive. The examiner respectfully disagrees with the applicant's arguments as

presented. The prior art reference Holcomb teaches determining the validity of different

parameters such as motion vectors. Holcomb does not teach counting the number of

motion vectors. However counting the number of motion vectors is well known in the art

as taught by Kim. As to Applicant's arguments regarding the Kim reference the

Examiner respectfully disagrees. Regarding Applicant's argument concerning

"comprises one or more bits, each of which are associated with a corresponding one or

more motion vector registers, wherein the one or more bits are in a particular stat,

based on whether the corresponding motion vector register stores a motion vector." Kim

teaches the limitations as claimed. [col. 5 line 57- col. 6 lines 20; Abstract; Col. 1 Lines

44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; col. 5 line 57- col. 6 lines 20]

2. With respect to claim 12 the amendment has been fully considered and the

objection of claim 12 has been withdrawn.

## Claim Objections

3. Claim 12 is objected to because of the following informalities: claim 12 is

dependant upon claim 10 which has been cancelled. Appropriate correction is required.

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## Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claims 1, 4, 8-9, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holcomb et al. US 2005/0105883 in view of Kato US 5,701,164.
- 6. As to claim 1, Holcomb teaches an input for receiving parameters, the parameters comprising a picture type indicator for indicating a type of a picture; [fig. 2; fig. 6; ¶ 0095 ¶ 0049] and logic for determining whether the parameters received by the input are valid, wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is progressive or interlaced. [fig. 6; ¶ 0095]

Holcomb does not explicitly the logic determines the number of motion vectors received by the input.

Kato teaches counting the number of motion vectors received by the input. [abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kato with the device of Holcomb allowing for improved coding.

7. As to claim 4, Holcomb (modified by Kato) teaches a control register for providing the type of pictures and indicating the number of motion vectors received to the logic.

[Holcomb - ¶ 0039; ¶0095; Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

8. As to claim 8, Holcomb teaches receiving parameters <u>at a video decoder</u>, the parameters comprising a picture type indicator for indicating a type of a picture [fig. 2; fig. 6; ¶ 0095 ¶ 0049] and determining the validity of the parameters, wherein the determining whether the parameters received by the input are valid based on the picture type indicator, whether the picture is interlaced or progressive, whether the picture is frame predicted or field. [fig. 6; ¶ 0008; ¶ 0082; ¶ 0095-0096]

Holcomb does not explicitly the logic determines the number of motion vectors received by the input.

Kato teaches counting the number of motion vectors received by the input. [abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kato with the device of Holcomb allowing for improved coding.

- 9. As to claim 11, Holcomb (modified by Kato) teaches determining the validity of the parameters further comprises determining that the parameters are invalid if the type of picture is an I-picture and any motion vectors are received. [Holcomb fig. 2; fig. 6; ¶ 0095 ¶ 0049 Kato abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]
- 10. As to claim 12, Holcomb (modified by Kato) teaches determining the validity of the parameters further comprises determining that the parameters are invalid if the

control register indicates that the type of picture is a B-picture and less than two of the one or more bits are in the particular state. [Holcomb - fig. 6; ¶ 0095; Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

- 11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Holcomb et al. US 2005/0105883 in view of Kato US 5,701,164 further in view of Drescher US 7,577,818.
- 12. As to claims 2, Holcomb (modified by Kato) teaches the limitations of claim 1.

Holcomb (modified by Kato) does not explicitly teach an arithmetic logic unit for calculating one or more addresses depending on whether the logic determines that the addresses are valid.

Drescher teaches an arithmetic logic unit for calculating one or more addresses depending on whether the logic determines that the addresses are valid. [col. 1 lines 14-29]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the address calculation of Drescher with the device of Holcomb modified Kato allowing for optimized and efficient coding.

13. Claim 13-15, 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holcomb et al. US 2005/0105883 in view of Kato US 5,701,164 further in view of Drescher US 7,577,818.

14. As to claim 13, Holcomb teaches a video decoder for decoding macroblocks, said video decoder comprising: a processor for decoding a set of parameters, [fig. 3] a picture type parameter indicating a type of picture; [fig. 6; ¶ 0095] the logic determines whether the parameters received by the input are valid based on the picture type indicator received by the input, [fig. 6; ¶ 0095] whether the picture is frame predicted, field predicted. [fig. 6; ¶ 0008; ¶ 0082; ¶ 0095-0096]

Holcomb does not explicitly teach calculating addresses associated with motion vectors if the set of parameters are valid; a video request manager for fetching reference pixels at the addresses calculated by the motion vector address computer, if the motion vector address computer determines that the set of parameters are valid, motion vectors indicating reference pixels associated with the macroblock and as to the logic determines whether the parameters received by the input are valid based on the picture type indicator whether the picture is frame predicted, field predicted, dual prime or 16x8 motion compensation and the number of motion vectors received by the input, motion vectors indicating reference pixels associated with the macroblock.

Kato teaches whether the picture is dual prime or 16x8 motion compensation [col. 31 lines 22-28; col. 32 lines 13-15, 40-42] counting the number of motion vectors received by the input. [abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kato with the device of Holcomb allowing for improved coding.

Holcomb modified by Kato does not explicitly teach calculating addresses

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associated with motion vectors if the set of parameters are valid; a video request

manager for fetching reference pixels at the addresses calculated by the motion vector

address computer, if the motion vector address computer determines that the set of

parameters are valid, motion vectors indicating reference pixels associated with the

macroblock and motion vectors indicating reference pixels associated with the

macroblock.

Drescher teaches calculating addresses associated with motion vectors if the set

of parameters are valid. [col. 1 lines 14-29]

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to incorporate the address calculation of Drescher with the device

of Holcomb modified Kato allowing for optimized and efficient coding.

Holcomb (modified by Kato and Drescher) does not explicitly teach a video

request manager for fetching reference pixels at the addresses calculated by the motion

vector address computer, if the motion vector address computer determines that the set

of parameters are valid.

Wise a video request manager for fetching reference pixels at the addresses

calculated by the motion vector address computer, if the motion vector address

computer determines that the set of parameters are valid. [Pq. 31 ¶ 0400; Pq. 163 ¶

2587]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Wise with the device of Holcomb (modified by Kato and Drescher) allowing for enhanced efficiency.

Holcomb (modified by Kato, Drescher and Wise) does not explicitly teach motion vectors indicating reference pixels associated with the macroblock.

Kim teaches motion vectors indicating reference pixels associated with the macroblock. [Col. 1 Lines 44-57]

It would have been obvious to one of ordinary one of ordinary skill in the art to combine the teachings of Kim with the coding device of Holcomb (modified by Kato, Drescher and Wise) allowing for reduction of errors in image reproduction and the improved speed of decoding.

- 15. As to claim 14, Holcomb (modified by Kato, Drescher, Wise and Kim) teaches an input for receiving parameters, the parameters comprising a picture type indicator for indicating a type of a picture; [Holcomb fig. 6; ¶ 0095] and logic for determining whether the parameters received by the input are valid. [Holcomb fig. 6; ¶ 0095]
- 16. As to claim 15, Holcomb (modified by Kato, Drescher, Wise and Kim) teaches an arithmetic logic unit for calculating one or more addresses depending on whether the logic determines that the addresses are valid. [Drescher col. 1 lines 14-29]
- 17. As to claim 17, Holcomb (modified by Kato, Drescher, Wise and Kim) teaches a control register for providing the type of pictures [Holcomb fig. 6; ¶ 0095] and

indicating the number of motion vectors received to the logic. [Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the address calculation of Drescher with the device of Holcomb modified Kato allowing for optimized and efficient coding.

- 18. As to claim 21, Holcomb (modified by Kato, Drescher, Wise and Kim) teaches wherein the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector. [Kim Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; Kato abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]
- 19. Claim 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holcomb et al. US 2005/0105883 in view of Kato US 5,701,164 further in view of Wise et al. (Wise) US 2003/0156652 A1.
- 20. As to claim 9, Holcomb (modified by Kato) teaches the limitations of claim 8.

Holcomb (modified by Kato) does not explicitly teach fetching pixels from the one or more addresses.

Wise teaches fetching pixels from the one or more addresses. [Pg. 163 ¶ 2587]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Wise with the device of Holcomb (modified by Kato) allowing for enhanced efficiency.

- 21. Claims 5-7 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holcomb et al. US 2005/0105883 in view of Kato US 5,701,164 in view of Wise et al. (Wise) US 2003/0156652 A1 further in view of Kim et al. (Kim) US 6,215,823 B1.
- 22. As to claim 5, Holcomb (modified by Kato) teaches the limitations of claim 4.

Holcomb (modified by Kato) does not explicitly teach one or more motion vector registers for storing motion vectors received by the input; control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector.

Wise teaches one or more motion vector registers for storing motion vectors received by the input; [Wise - Pg. 51 ¶ 0682 Table A.3.2]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Wise with the device of Holcomb (modified by Kato) allowing for enhanced efficiency.

Holcomb (modified by Kato and Wise) does not explicitly teach the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a

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particular state, based on whether the corresponding motion vector register stores a motion vector.

Kim teaches the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector. [Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; col. 5 line 57- col. 6 lines 20]

It would have been obvious to one of ordinary skill in the art to combine the teachings of Kim with the coding device of Holcomb (modified by Kato and Wise) allowing for reduction of errors in image reproduction and the speed of decoding.

- 23. As to claim 6, Holcomb (modified by Kato, Wise and Kim) teaches the logic determines that the parameters are invalid if the control register indicates that the type of picture is an I-picture and any of the one or more bits are in the particular state. [Holcomb fig. 6; ¶ 0095; Kato abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41; Kim Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; col. 5 line 57- col. 6 lines 20; Abelard col. 2 lines 50-56; col. 4 lines 25-34, 49-58]
- 24. As to claim 7, Holcomb (modified by Kato, Wise and Kim) teaches the logic determines that the parameters are invalid if the control register indicates that the type of picture is a B- picture and less than two of the one or more bits are in the particular state. [Holcomb fig. 6; ¶ 0095; Kato abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6

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Lines 8-12; col. 5 line 57- col. 6 lines 20; Abelard - col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

- 25. As to claim 18, Holcomb (modified by Kato, Wise and Kim) teaches one or more motion vector registers for storing motion vectors received by the input; [Wise Pg. 51 ¶ 0682 Table A.3.2] and wherein the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector. [Kim Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; Kato abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]
- 26. As to claim 19, Holcomb (modified by Kato, Wise and Kim) teaches the logic determines that the parameters are invalid if the control register indicates that the type of picture is an I-picture and any of the one or more bits are in the particular state. [Holcomb fig. 6; ¶ 0095; Kim Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; Abelard col. 2 lines 50-56; col. 4 lines 25-34, 49-58]
- 27. As to claim 20, Holcomb (modified by Kato, Wise and Kim) teaches the logic determines that the parameters are invalid if the control register indicates that the type of picture is a B-picture and less than two of the one or more bits are in the particular state. [Holcomb fig. 6; ¶ 0095; Kim Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; Abelard col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

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Conclusion

28. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to ANNER HOLDER whose telephone number is

(571)270-1549. The examiner can normally be reached on M-W, M-W 8 am-3 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Joseph Ustaris can be reached on 571-272-7383. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

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Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anner Holder/

Examiner, Art Unit 2483

/Tuna Vo/

Primary Examiner, Art Unit 2483